Image Pickup Apparatus

BACKGROUND OF THE INVENTION

Field of the Invention

The present invention relates to an image pickup apparatus for picking up an object image.

Related Background Art

Conventional solid-state image pickup elements are mainly classified into CCD-type elements and CMOS-type elements. Examples of CCD-type elements are an interline CCD (IL-CCD) and frame transfer CCD (FT-CCD).

An interline CCD comprises a plurality of photoelectric conversion units, vertical CCDs, transfer gates for transferring signal charges in the photoelectric conversion units to the vertical CCDs, a horizontal CCD for horizontally transferring the charges from the vertical CCDs, and a floating diffusion amplifier (FD-Amp). A frame transfer CCD comprises photoelectric conversion units, a storage unit to which charges in the photoelectric conversion units are transferred (frame-shifted), a horizontal transfer unit for horizontally transferring the charges from the storage unit, and a floating diffusion amplifier (FD-Amp). Fig. 11 shows an IL-CCD as a typical example of a CCD-type solid-state image pickup element.

As shown in Fig. 11, an IL-CCD comprises

photoelectric conversion units (PDs) 70, vertical CCDs (V-CCDs) 71 for temporarily storing charges from the photoelectric conversion units 70, a horizontal CCD (H-CCD) 72 for receiving the charges from the vertical CCDs 71 and transferring the charges in the horizontal direction, and a floating diffusion amplifier (FD-Amp) 73 serving as an output amplifier for converting the charges from the horizontal CCD 72 into a voltage.

The CCD has low noise level because signal charges are completely transferred to the FD-Amp on the output side. In addition, the pixel size can be made small because of the simple pixel structure. Today, however, the number of pixels in a sensor for a digital camera reaches several millions for higher quality, and high-speed drive is indispensable in an HD camera. For this reason, the power consumption of a horizontal CCD drive circuit is high (up to CfV_2). Although a CDS circuit for reducing reset noise in an FD-Amp requires a sampling accuracy on the order of nsec, that sampling accuracy cannot be ensured because of the mass production and the wide range of use conditions (temperature and a variation in voltage). Hence, a low-noise CCD can hardly be implemented.

In a CMOS sensor, as shown in Fig. 12, each pixel unit 80 comprises a photoelectric conversion unit PD and a MOS transistor serving as a pixel amplifier. The pixels are selected and driven by a random-accessible

vertical scanning circuit 81 and horizontal scanning circuit 85, resulting in functional advantage. Charges in each pixel unit 80 are converted into a voltage by the pixel amplifier, output to a clamp circuit 83 through a vertical signal line 82, and after noise removal from the pixel unit amplifier by the clamp circuit 83, output to a horizontal signal line 84. The signals are sequentially output by the horizontal scanning circuit 85 from the horizontal signal line 84 through an amplifier (Amp) 86. Since a CMOS sensor sequentially selects and outputs each pixel signal by the horizontal scanning circuit 85, unlike charge transfer as in a CCD, the power consumption is low. However, since the number of elements of each pixel unit is large, it is difficult to reduce the pixel size.

As described above, a CCD is advantageous in increasing the number of pixels but disadvantageous in high-speed drive and power consumption. Conversely, a CMOS sensor is disadvantageous in increasing the number of pixels but advantageous in high-speed drive and power consumption.

SUMMARY OF THE INVENTION

It is an object of the present invention to provide an image pickup apparatus suitable to increase the number of pixels and capable of high-performance

function, power consumption reduction, and high-speed drive.

In order to achieve the above object, according to an aspect of the present invention, there is provided an image pickup apparatus comprising:

a solid-state image pickup element formed on a single semiconductor chip, the solid-state image pickup element including:

photoelectric conversion units arranged two-dimensionally;

a plurality of CCDs adapted to transfer charges generated by the photoelectric conversion units arranged two-dimensionally, each of the plurality of CCDs being arranged correspondingly to each line of photoelectric conversion units;

a plurality of charge detection circuits adapted to detect the charges from the plurality of CCDs and supplying corresponding signal levels, each of the plurality of charge detection circuits being arranged correspondingly to each CCD;

a common output line to which signals from the plurality of charge detection circuits are sequentially output;

a plurality of transfer transistors adapted to transfer the signals from the plurality of charge detection circuits to the common output line; and

a scanning circuit adapted to control the

plurality of transfer transistors to sequentially output the signals from the plurality of charge detection circuits to the common output line.

According to another aspect of the present invention, there is provided an image pickup apparatus comprising:

a solid-state image pickup element formed on a single semiconductor chip, the solid-state image pickup element including:

photoelectric conversion units arranged two-dimensionally;

a plurality of CCDs adapted to transfer charges generated by the photoelectric conversion units, each of the plurality of CCDs being arranged correspondingly to each line of photoelectric conversion units;

a plurality of charge detection circuits adapted to detect the charges from the CCDs and supplying corresponding signal levels, each of the plurality of charge detection circuits being arranged correspondingly to each CCD; and

a plurality of A/D conversion circuits adapted to convert the signals from the charge detection circuits into digital signals, each of the A/D conversion circuits being arranged correspondgly to each charge detection circuit.

The above and other objects, features, and advantages of the present invention will become

apparent from the following description in conjunction with the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 is a schematic view showing a solid-state image pickup element according to the first embodiment of the present invention;

Fig. 2 is a schematic view of a charge detection circuit and signal processing circuit shown in Fig. 1;

Fig. 3 is an operation timing chart of the charge detection circuit and signal processing circuit shown in Fig. 2;

Fig. 4 is a view showing a solid-state image pickup element according to the second embodiment of the present invention;

Figs. 5A and 5B are explanatory views of random access drive according to the third embodiment of the present invention;

Fig. 6 is a block diagram of an equivalent circuit having a charge detection circuit and A/D conversion circuit unit according to the fourth embodiment of the present invention;

Fig. 7 is a timing chart for explaining the operation shown in Fig. 6;

Fig. 8 is a schematic circuit diagram showing connection between a vertical CCD and a charge detection circuit and A/D conversion circuit according

to the fourth embodiment of the present invention;

Figs. 9A and 9B are sectional views showing the structure of a solid-state image pickup element according to the fifth embodiment of the present invention;

Fig. 10 is a block diagram showing a case wherein the solid-state image pickup element of any one of the first to fifth embodiments is applied to a "digital still camera";

Fig. 11 is a schematic view of an IL-CCD;

Fig. 12 is a schematic view of a CMOS sensor; and

Fig. 13 is a view showing a structure in which an inverter unit is separated by a deep well.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

The embodiments of the present invention will be described below in detail with reference to the accompanying drawings. An arrangement using an interline CCD (IL-CCD) will be described here. The present invention can also be applied to a frame transfer CCD. In that case, charges from a storage unit are output to a charge detection circuit.

Fig. 1 is a schematic view showing a solid-state image pickup element according to the first embodiment of the present invention. Object light is photoelectrically converted by photodiodes (PDs) 1 each serving as a photoelectric conversion unit. The

photodiodes 1 are arrayed in a matrix form as pixels P_{11}, P_{12}, P_{13},..., P_{21}, P_{22}, P_{23},..., P_{31}, P_{32}, P_{33},.... Charges photoelectrically converted by the photodiodes 1 are transferred to vertical CCDs 2 through transfer gates. The charges transferred to the vertical CCDs 2 are transferred to charge detection circuits 3 and converted into a voltage at once every horizontal period. The interline CCD unit is formed from the photodiodes 1 and vertical CCDs 2. Unlike the conventional interline CCD shown in Fig. 11, signal charges from the vertical CCDs are transferred (not to the horizontal CCD) to the charge detection circuits 3.

The signal voltage is output to a horizontal signal line 5 in accordance with a pulse from a horizontal scanning circuit 4 and guided to an image signal processing circuit (not shown) on the output side through an output amplifier 6.

The output signal from each charge detection circuit 3 may be directly read out. Alternatively, a signal processing means for executing signal processing such as noise removal or A/D conversion may be provided on the output side of each charge detection circuit 3 and the signal may be output by the horizontal scanning circuit 4.

The solid-state image pickup element shown in Fig. 1 is formed on a single semiconductor chip.

Fig. 2 is a schematic view of the charge detection

circuit and signal processing circuit shown in Fig. 1. The charge detection circuit comprises a charge detection amplifier (FD-Amp; floating diffusion amplifier) having a gate to which signal charges from the vertical CCD are transferred, and a reset transistor TR for resetting the gate of the charge detection amplifier. The signal processing circuit comprises a clamp capacitor Cp for removing noise, a transistor Tp, storage capacitors C_{S1} and C_{S2} for storing signals after noise removal, transfer transistors T_{S1} and T_{S2} for connecting the clamp capacitor Cp to the storage capacitors C_{S1} and C_{S2}, and transistors T_{C1} and T_{C2} for outputting signals from the storage capacitors C_{S1} and C_{S2} to horizontal signal lines 5_1 and 5_2. These components form a charge detection/signal processing block 100.

The vertical CCD 2 transfers charges to the charge detection amplifier (FD-Amp; floating diffusion amplifier) through a transfer gate TG every horizontal period in accordance with a drive pulse ϕVn. In the charge detection amplifier (FD-Amp), reset noise is generated by a parasitic capacitance and the reset transistor TR for removing residual voltage (charges) in the gate unit. In addition, the offset voltage fluctuates among the charge detection amplifiers (FD-Amps). To remove these noise components, the noise is clamped by the clamp capacitor Cp before the charges

are transferred from the vertical CCD 2 to the charge detection amplifier (FD-Amp).

After this clamp, the transfer gate TG is turned on to transfer the charges in the vertical CCD 2 (signal charges from the pixels P_{11}, P_{12}, P_{13},...) to the gate unit of the charge detection amplifier (FD-Amp) and converted into a voltage by its parasitic capacitance. The above-described reset noise and offset voltage are superposed on the output signal voltage from the charge detection amplifier. Since the noise components are clamped by the clamp capacitor Cp, the noise is consequently removed at the output terminal of the clamp capacitor Cp, and only the signal voltage is stored in the storage capacitor C_{S1}.

With the same operation, the next charges in the vertical CCD 2 (signal charges from the pixels P_{21}, P_{22}, P_{23},...) are converted into a voltage and, after noise removal, stored in the storage capacitor C_{S2}. Pixel signals S_{01} and S_{02} of two rows which are stored in the storage capacitors C_{S1} and C_{S2} are sequentially transferred to the horizontal signal lines 5_1 and 5_2 in accordance with a scanning pulse from the horizontal scanning circuit 4.

Fig. 3 is an operation timing chart of the charge detection circuit and signal processing circuit shown in Fig. 2.

As shown in Fig. 3, first, the drive pulse ϕVn

goes high during a period T_1 to transfer charges to the vertical CCD 2 on the input side of the transfer gate TG. During a period T_2, a power supply voltage Vcc of the charge detection amplifier (FD-Amp) is applied, a signal ϕ_C goes high to reset the gate of the charge detection amplifier (FD-Amp), a signal ϕ_P goes high to turn on the transistor Tp, the output terminal of the clamp capacitor Cp is clamped to the reference voltage, and signals ϕ_{S1} and ϕ_{S2} go high to reset the residual charges in the storage capacitors C_{S1} and C_{S2}. At this time, reset noise and offset voltage components are clamped by the clamp capacitor Cp.

During a period T_3, a signal ϕ_T goes high to turn on the transfer gate TG and transfer the signal charges to the gate portion of the charge detection amplifier. The above-described reset noise and offset voltage are superposed on the output signal voltage from the charge detection amplifier. However, the noise is consequently removed at the output terminal of the clamp capacitor Cp, and the signal ϕ_{S1} goes high, so that the pixel signal of a row V_1, from which noise has been removed, is stored in the storage capacitor C_{S1}.

During periods T_4 and T_5, with the same operation as in the periods T_2 and T_3, charges in the vertical CCD 2 are transferred to the next cell. In a state wherein the power supply voltage Vcc of the charge detection amplifier (FD-Amp) is applied, the signal ϕ_C goes high

to reset the gate of the charge detection amplifier (FD-Amp), and the signal ϕ_P goes high to clamp the output terminal of the clamp capacitor Cp to the reference voltage. The signals ϕ_T and ϕ_{S2} go high so that the pixel signal of a row V_2, from which noise has been removed, is stored in the storage capacitor C_{S2}.

After the end of the period T_5, the power supply voltage Vcc of the charge detection amplifier is turned off to prevent power consumption.

As described above, since the charge detection amplifier operates at a low speed in one horizontal scanning period, the frequency bandwidth is small. For this reason, noise generated in the amplifier is much smaller than in the output amplifier of a general CCD. In addition, because of low-frequency drive, no problem is posed in noise removing operation (CDS), i.e., clamp operation. To increase the 1/f noise reduction effect of the FD-Amp, the time required for reset operation of the FD-Amp and charge transfer from the vertical CCD is preferably short.

The signals stored in the storage capacitors C_{S1} and C_{S2} are sequentially output during a next period T_6 in accordance with a scanning pulse ϕHmn (ϕH_{01}, ϕH_{02}, ϕH_{03},...) from the horizontal scanning circuit 4. That is, since the signal is selected and output on the each pixel signal basis, the power consumption of the horizontal scanning circuit is low. In addition, since

pixel signals of two rows can be simultaneously output, high-speed drive can be performed. If drive at a higher speed is necessary, the number of memories (storage capacitors) is increased to execute multiple-line output.

Fig. 4 shows a solid-state image pickup element according to the second embodiment of the present invention. Circuits in a charge detection/signal processing block 100, which are identical to those in Fig. 2, are not illustrated in Fig. 4.

In this embodiment, charges in a plurality of vertical CCDs 2 are sequentially output using a common charge detection amplifier. Signals ϕ_{T1} and ϕ_{T2} are sequentially set to H level to turn on transfer gates T_{G1} and T_{G2} to sequentially control charge transfer from vertical CCDs of two columns to the charge detection amplifier whereby pixel signals of two columns are stored in storage capacitors C_{S1} and C_{S2} and output. In this embodiment, since the charge detection circuit and signal processing circuit can be formed in the width of two pixels, the chip area can be decreased.

The signal processing circuit can have a programmable gain amplifier, A/D conversion circuit, and for a color sensor, a white balance circuit, and the like.

Figs. 5A and 5B are explanatory views of the third embodiment related to random access drive. This

embodiment has the same arrangement as described above except a horizontal scanning circuit 4, and as its characteristic feature, the solid-state image pickup element is a random-accessible solid-state image pickup element. Fig. 5A is a view showing an image pickup surface, and Fig. 5B is a timing chart of an image read from an image pickup area A.

An image pickup area includes the image pickup areas A and B. In the prior art, drive is performed using almost the same frequency for both the vertical and horizontal scanning periods. In fact, high-speed drive can be performed when only the image pickup area A that should be read out is read out. In the conventional CCD, it is difficult to read out the image pickup area A to be read out at a high speed. In the embodiment of the present invention, during an unnecessary image pickup period V_A (V_C) in the vertical direction, the vertical CCD is driven at a high speed to remove unnecessary charges by a reset transistor TR of the charge detection amplifier. During an unnecessary image pickup period H_A (H_C) in the horizontal direction, a random-accessible horizontal scanning circuit is arranged to execute scanning to output a signal only during a period H_B. That is, a decoder or a shift register which is divided into a plurality of areas and can start on each area basis is used. As a result, only the image signal in the image

pickup area A can be read out. For this reason, high-speed drive can be achieved, and the power consumption can be reduced because the unnecessary image pickup area is not driven.

More developed random access can be realized by a CCD capable of selecting a pixel row. As a known example, an element is disclosed in the Institute of Image Information and Television Engineers technical report TEBS 101-6 ED 841. This known example is called a charge sweep device in which pixel row selection is driven by a vertical TG-SCANNER. When such a charge sweep device and the charge detection amplifier and signal processing circuit according to this embodiment are combined, the technological advantages of this embodiment can be expected.

As a characteristic feature of the fourth embodiment, an A/D conversion circuit unit is prepared for each column. Fig. 6 is a block diagram of an equivalent circuit having a charge detection circuit and sequential-comparison-type A/D conversion circuit unit. A D/A converter receives DA output range switching information used to switch the range of the ramp-shaped reference voltage.

Referring to Fig. 6, the circuit comprises a vertical CCD 2, a transfer gate 42 for transferring signal charges from the vertical CCD 2 to the gate of an FD-Amp (floating diffusion amplifier) 43, a

selection transistor 44, a reset transistor 45, a current supply transistor 46 for storing, as a voltage, the output current from the FD-Amp 43 by a switch 47 and storage capacitor 48 and outputting the voltage while converting it into a current, a comparator 51 for detecting the difference between the output current from the current supply transistor 46 and the output current from the FD-Amp 43 through the selection transistor 44, a counter 50 for counting the output from the comparator 51, and a D/A converter 49 for outputting a voltage to the source (main electrode) terminal of the FD-Amp 43 in accordance with a digital signal output from the counter 50. The D/A converter 49 receives DA output range switching information to switch the range of the ramp-shaped reference voltage to be output from the D/A converter 49 such that the pixel signal has an optimum value within the A/D input voltage range.

A method of obtaining a signal voltage by signal charges from the vertical CCD after the FD-Amp is reset in the above arrangement will be described as an example with reference to the timing chart shown in Fig. 7. The description below will be made while assuming that the transistors 42, 43, 44, and 45 shown in Fig. 6 are PMOS transistors, and the transistor 46 is an NMOS transistor. The D/A converter 49 is set to output a high potential (V_{HD}). Assume that the counter

50 is reset and no count operation is being performed. A signal ϕ_C is set to "L" level (pulse 201) to turn on the reset transistor 45 to reset the gate terminal of the FD-Amp 43 to a predetermined potential. Simultaneously, a signal ϕ_X is set to "L" level (pulse 202) to turn on the selection transistor 44 and also turn on the switch 47. The output current from the FD-Amp 43 at the time of reset is stored in the storage capacitor 48 as a gate voltage generated when the gate and drain of the transistor 46 short-circuit (the comparison reference voltage is stored). After that, the transistors 45 and 44 and switch 47 are turned off, and a signal ϕ_T is set to "L" level (pulse 203) to turn on the transfer gate 42 to transfer signal charges from the vertical CCD to the gate terminal of the FD-Amp 43. If the gate potential at this time is lower than that at the time of reset, the output current from the FD-Amp 43 has a larger value than at the time of reset. The transistor 46 receives the voltage from the storage capacitor 48 and outputs the current when the FD-Amp 43 is reset. When the signal ϕ_X is set to "L" level (pulse 204) to turn on the transistor 44 again, the input potential of the comparator 51 rises to a high potential (V_H). After that, the counter 50 is operated, and its digital output is amplified. The output voltage from the D/A converter 49 that receives the output from the counter 50 gradually decreases (assume

that the D/A converter 49 generates a negative analog output voltage with respect to the digital input signal). At certain time, the output current from the FD-Amp 43 becomes equal to that from the transistor 46, and the input voltage to the comparator 51 abruptly decreases. Upon detecting that change, the count operation of the counter 50 is stopped.

The digital value that has changed during a period from the start to the end of counting by the counter 50 equals to the difference between the gate potential of the FD-Amp 43 at the time of reset and the potential when the signal charges are transferred. In this way, A/D conversion is executed correspondingly to the difference.

Fig. 8 is a schematic circuit diagram showing connection between the vertical CCD and the charge detection circuit and A/D conversion circuit. The same reference numerals as in Fig. 6 denote the same members in Fig. 8.

The signal charges from the vertical CCD 2 are input to the gate of the FD-Amp 43, converted into digital data by the counter 50, sequentially selected by a data selector 52, and output as A/D-converted data.

Figs. 9A and 9B are sectional views showing the structure of a solid-state image pickup element according to the fifth embodiment. Fig. 9A is a

sectional view showing the structure of a photoelectric conversion unit, vertical CCD, and channel stop.

Fig. 9B is a sectional view showing the structure of an inverter unit that forms part of a signal processing circuit.

As shown in Fig. 9A, a unit pixel is formed from a PD region serving as a photoelectric conversion unit, a transfer gate region for transferring charges, a vertical CCD region, and a channel stop region. These regions are formed in a p-well 65 formed on an n-substrate 60. In the PD region, a dark current is reduced by a p^+-layer 67 on the surface. In the vertical CCD region, a p-layer 68 is formed under an n-layer 69 to reduce an increase and smearing in transfer charge amount. In the transfer gate region, control is executed to transfer photocharges from the PD to the vertical CCD. The solid-state image pickup element also has a microlens 61 for focusing light in the PD region, a light-shielding layer 62, a gate electrode 63 made of polysilicon, and an SiO_2 layer 64.

As shown in Fig. 9B, in the inverter unit as part of the signal processing circuit, a p-well and n-well are formed on the n-substrate 60 to form an NMOS transistor and PMOS transistor.

Well separation between the CCD unit and the signal processing circuit unit is preferably done from the charge detection circuit unit. This is because the

signal processing circuit unit generates pulse noise due to high-speed signal transfer or the logic circuit. To prevent noise from propagating from the noise source to the CCD unit, the CCD unit and signal processing circuit are separated by the well. For some application purposes, the charge detection circuit unit may be formed in the CCD well. Since the charge detection circuit unit has a function of converting signal charges into a voltage every horizontal period and therefore operates at a low speed, it generates little noise. Fig. 13 shows a structure in which the inverter unit is separated by a deep well. When the inverter unit is completely separated from the sensor unit, noise from the inverter unit can be more effectively shielded. The solid-state image pickup element of this embodiment can have any one of the equivalent circuits of the first to fourth embodiments.

The sixth embodiment wherein the solid-state image pickup element of any one of the above-described first to fourth embodiments is applied to a digital still camera (image pickup apparatus) will be described in detail with reference to Fig. 10.

Referring to Fig. 10, the camera has a barrier 111 serving as the protection and main switch of a lens, a lens 112 for forming an optical image of an object onto a solid-state image pickup element 114, an iris 113 for changing the amount of light transmitted through the

lens 112, the solid-state image pickup element 114 for receiving the object image formed by the lens 112 to output an image signal, an image pickup signal processing circuit 115, an A/D converter 116 for executing A/D conversion of the image signal output from the image pickup signal processing circuit 115, a signal processing unit 117 for executing various kinds of correction operations for the image data output from the A/D converter 116 or compressing the data, a timing generation unit 118 for outputting various kinds of timing signals to the solid-state image pickup element 114, image pickup signal processing circuit 115, A/D converter 116, and signal processing unit 117, a system control and operation unit 119 for executing various kinds of operations and controlling the entire still video camera, a memory unit 120 for temporarily storing the image data, an interface unit 121 for recording/reading out the image data on/from a recording medium, a detachable recording medium 122 such as a semiconductor memory for recording or reading out image data, and an interface unit 123 for communication with an external computer or the like.

The operation of the still video camera with the above-described arrangement in the phototaking mode will be described next. When the barrier 111 is opened, the main power supply is turned on, the power supply of the control system is turned on next, and

finally, the power supply of the image pickup system circuit such as the A/D converter 116 is turned on. To control the exposure amount, the system control and operation unit 119 sets the iris 113 in the full-aperture state. The signal output from the solid-state image pickup element 114 is converted by the A/D converter 116 and input to the signal processing unit 117. The system control and operation unit 119 executes calculation for exposure on the basis of the data. The brightness is determined on the basis of the result of photometry, and in accordance with the result, the system control and operation unit 119 controls the iris.

On the basis of the signal output from the solid-state image pickup element 114, a high-frequency component is extracted, and the distance to the object is calculated by the system control and operation unit 119. After that, the lens is driven, and it is determined whether an in-focus state is obtained. If it is determined that no in-focus state is obtained, the lens is driven again, and distance measurement is performed. After confirming the in-focus state, actual exposure starts.

When exposure is ended, the image signal output from the solid-state image pickup element 114 is A/D-converted by the A/D converter 116, passes through the signal processing unit 117, and is written in the

memory unit by the system control and operation unit 119.

After that, the data stored in the memory unit 120 is recorded on the detachable recording medium 122 such as a semiconductor memory through the recording medium control I/F unit 121 under the control of the system control and operation unit 119. The image data may be directly input to a computer or the like through the external I/F unit 123 to process the image.

As has been described above in detail, according to this embodiment, a sensitive image pickup apparatus capable of high-performance function, high-speed drive, and power consumption reduction can be provided.

Many widely different embodiments of the present invention may be constructed without departing from the spirit and scope of the present invention. It should be understood that the present invention is not limited to the specific embodiments described in the specification, except as defined in the appended claims.